IN THE DRAWINGS

Please amend the drawings by substituting the enclosed 3 sheets of drawings containing Figures 1, 2A, 2B, and 3 for the 3 sheets of drawings containing Figures 1, 2A, 2B, and 3 previously submitted on August 18, 2003.

Figures 1 and 3 are hereby amended to delete the arrow coming into box 11 and the arrow coming out of box 10. Figure 2A is hereby amended such that the reference numerals 21 and 22 are now arrows pointing to different regions of the layout in Figure 2A.

REMARKS

Claims 1-20 were presented for examination and were pending in this application. In an Official Action dated August 5, 2005, claims 1-20 were rejected. Claims 1-20 are canceled herein without prejudice or disclaimer, and new claim 21 is added. New claim 21 is supported by FIG. 3 and its accompanying description in the specification, and thus this amendment does not introduce new matter.

Objection to the Drawings

The Examiner objected to Figures 1 and 3, because the there is no indication of where the inputs to box 11 come from and where the outputs from box 10 go to. The arrow coming into box 11 and the arrow coming out of box 10 in Figures 1 and 3 were deleted herein, and thus this objection is overcome.

The Examiner also objected to Figure 2A, because the reference numerals 21 and 22 point to the same element. Figure 2A is amended herein such that the reference numerals 21 and 22 are now arrows pointing to different regions of the layout in Figure 2A, i.e., the reference numeral 21 for a densely packed region and the reference numeral 22 for a region with only one isolated wire, as is consistent with the description for Figure 2A. See page 7, lines 11-13 of the specification. Thus, this objection is also overcome.

Approval of the proposed amendments to the drawings is respectfully requested. The Examiner is also requested to explicitly indicate his approval in the next communication.

Claim Objections

Claim 1 was objected to because it contains indefinite languages, "may be" before "executed independently" and "the" before "second modified circuit." Claim 1 is canceled herein, and thus this objection is overcome.

Claims 2, 5, 6, and 13 were objected to because they contain limitations not disclosed by the specification: "storage repository" in claims 2 and 13, "first and second processors" in claim 5, and "layout sub-divisions" in claim 6. Claims 2, 5, 6, and 13 are canceled herein, and thus these objections are overcome.

Claim Rejections under 35 USC §112, 1st Paragraph

Claim 1-13 were rejected as failing to comply with the written description requirement. Claims 1-13 are canceled herein, and thus these rejections are overcome.

Claim Rejections under 35 USC §102

Claims 1-20 were rejected as being anticipated by Kochpathcharin (US Patent Application Publication No. 2004/0181769 A1) and claims 14-16 were rejected as being anticipated by DeCamp (US Patent No. 6,063,132).

Claims 1-20 are canceled herein, and thus these rejections are overcome.

New Claim

New claim 21 recites:

"...performing a first circuit performance analysis on the layout;

incorporating manufacturing enhancements on the layout, the manufacturing enhancements including optical proximity correction;

performing a second circuit performance analysis on the layout using the layout with the manufacturing enhancements incorporated therein to generate a taped-out layout of the integrated circuit;

checking design-rules on the taped-out layout;

modifying the taped-out layout by performing the manufacturing enhancements on the taped-out layout using at least in part results of the first circuit performance analysis…"

As recited in claim 21, the method of generating a layout according to the present invention (i) incorporates manufacturing enhancements such as optical proximity corrections in the layout design stage of the layout, and also (ii) performs manufacturing enhancements on the taped-out layout such as optical proximity correction in the manufacturing stage, using at least in part the results of the first circuit performance analysis of the layout design stage. As a result, information gathered in the layout design stage of the layout and the manufacturing stage is exchanged, thereby significantly enhancing efficiency in layout design.

Kochpathcharin and DeCamp fail to disclose or even suggest incorporating manufacturing enhancements such as optical proximity corrections in the layout design stage of the layout and (ii) performing manufacturing enhancements on the taped-out layout such as optical proximity correction in the manufacturing stage, using at least in part the results of the circuit performance analysis of the layout design stage. Rather, Kochpathcharin merely discloses a method for modifying a customer specific reticle set design to a reticle set design that meets a user's process standard, and Decamp merely discloses a method of using a generate-and-verify computer program product to generate by repetitive passes a design rule checking program.

Therefore, it is respectfully submitted that new claim 21 is patentably distinct from Kochpathcharin and DeCamp.

Conclusion

In conclusion, it is respectfully submitted that the pending claim 21 is in condition for allowance. Favorable action is solicited.

Respectfully submitted,
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